We claim:

1. A bias generator, comprising:

a first node to receive a supply voltage; and

a single-stage source-follower to generate forward body bias for a local functional block based on a variation in the supply voltage received from the first node.

2. The bias generator of claim 1, wherein the single-stage source-follower includes:

first and second matched transistors to convert a first bias voltage into a second bias voltage based the supply voltage variation.

3. The bias generator of claim 2, further comprising:

a second node coupled between the first and second matched transistors, the second node outputting the second bias voltage as said forward body bias to the local functional block.

4. The bias generator of claim 3, wherein the first node is connected to a source of the first transistor, the second node is connected to a drain of the first transistor and a source of the second transistor, and gates of the first and second transistors are respectively connected to receive the first bias voltage and a reference voltage.

5. The bias generator of claim 4, wherein the single-stage source-follower converts the first bias voltage into the second bias voltage based on a difference between the supply voltage and the reference voltage.

6. The bias generator of claim 1, wherein the supply voltage is a supply voltage of the local functional block.

7. The bias generator of claim 1, wherein said forward body bias is NMOS body bias.

8. The bias generator of claim 1, wherein said forward body bias is PMOS body bias.

9. A circuit, comprising:

a central bias generator to generate a first bias voltage; and

a local bias generator including:

(a) a first node to receive a supply voltage, and

(b) a single-stage source-follower to convert the first bias voltage into a second bias voltage based on a variation in the supply voltage received from the first node.

10. The circuit of claim 9, wherein the single-stage source follower provides the second bias voltage as forward body bias to a local functional block.

11. The circuit of claim 10, wherein the supply voltage is a supply voltage of the local functional block.

12. The circuit of claim 9, wherein the single-stage source-follower includes:

first and second matched transistors that convert the first bias voltage into the second bias voltage based the supply voltage variation.

13. The circuit of claim 12, further comprising:

a second node coupled between the first and second matched transistors, the second node outputting the second bias voltage as forward body bias to a local functional block.

14. The circuit of claim 13, wherein the first node is connected to a source of the first transistor, the second node is connected to a drain of the first transistor and a source of the second transistor, and gates of the first and second transistors are respectively connected to receive the first bias voltage and a reference voltage.

15. The circuit of claim 14, wherein the single-stage source-follower converts the first bias voltage into the second bias voltage based on a difference between the supply voltage and the reference voltage.

16. The circuit of claim 14, wherein the central bias generator outputs the reference voltage.

17. The circuit of claim 16, wherein the central bias generator outputs the reference voltage as a shifted value.

18. The circuit of claim 9, wherein the second bias voltage provides NMOS forward body bias to a local functional block.

19. The circuit of claim 9, wherein the second bias voltage provides PMOS forward body bias to a local functional block.

20. A method, comprising:

receiving a supply voltage of a local functional block; and

generating forward body bias for the local functional block from a single-stage source-follower based on a variation in the supply voltage.

21. The method of claim 20, wherein generating the forward body bias includes:

converting a first bias voltage into a second bias voltage based on the supply voltage variation, said single-stage source-follower performing the conversion using first and second matched transistors.

22. The method of claim 20, wherein said converting includes:

converting the first bias voltage into the second bias voltage based on a difference between the supply voltage and a reference voltage.

23. The method of claim 20, wherein said forward body bias is NMOS body bias.

24. The method of claim 20, wherein said forward body bias is PMOS body bias.

25. A processing system, comprising:

a functional block;

a central bias generator to generate a first bias voltage; and

a local bias generator including:

(a) a first node to receive a supply voltage of the functional block, and

(b) a single-stage source-follower to convert the first bias voltage into a second bias voltage based on a variation in the supply voltage of the functional block.

26. The system of claim 25, wherein the single-stage source follower provides the second bias voltage as forward body bias to the functional block.

27. The system of claim 25, wherein the single-stage source-follower includes:

a second node; and

first and second matched transistors coupled to the second node, the first and second matched transistors convert the first bias voltage into the second bias voltage based the supply voltage variation.

28. The system of claim 27, wherein the first node is connected to a source of the first transistor, the second node is connected to a drain of the first transistor and a source of the second transistor, and gates of the first and second transistors are respectively connected to receive the first bias voltage and a reference voltage.

29. The system of claim 28, wherein the single-stage source-follower converts the first bias voltage into the second bias voltage based on a difference between the supply voltage and the reference voltage.

30. The system of claim 29, wherein the central bias generator outputs the reference voltage.